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RAYtheon RC 4805 EDE (?) 9.450 (81200) 50hz 40gg

OP-47 G N B/F ← 3°980

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AN-27

October 1, 1982

RC4805
High Speed Precision Latching Comparator Application Notes

RICEVUTO
26 NOV. 87

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Senior Design Engineer

RAYTHEON

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A High Speed Precision Latching Comparator

By

David J. Harris

Senior Design Engineer

Introduction

Voltage comparators are one of the commonest building blocks used by the system designer. Comparators with a wide variety of speed, accuracy and cost are available. New system designs emphasize higher speed and accuracy; yet cost and system power consumption can rarely be ignored.

The Raytheon 4805 voltage comparator offers the system designer new levels of performance at low cost and power. Response times of less than 30 nanoseconds and input errors substantially less than 0.01% in a 10 Volt system simplify designs that were difficult or impossible before. Table 1 lists the major features of the 4805.

The accuracy and speed of the 4805 doesn't depend on complex processing steps. A standard junction isolated, low voltage bipolar process is used. Aluminum schottky diodes are used which adds one masking step. The elimination of expensive processing steps such as ion implant, dielectric isolation, collector sinker, or dual layer metal makes the 4805 an easy and low cost part to produce. Innovative circuit design is the key to the 4805's performance.

A simplified schematic of the 4805 is shown in Figure 1. Three cascaded differential gain stages produce a small signal gain of 20,000. The first stages and the output device are schottky clamped. The TTL output is latched by applying a TTL "one" to pin 6, the latch enable.

The input characteristics of the 4805 are accomplished by careful layout, circuit design and wafersort trim. The first gain stage employs a technique that allows superbeta input current performance without superbeta transistors. This stage has two parallel differential pairs, Q1, Q2 and Q58, Q59. The tail current, I44, for the outside pair, Q1 and Q2, is only one-eighth the current of the internal pair, I60. The currents are summed by the common base transistor pair, Q3 and Q4. The stage gain and speed are that of a simple differential stage with a tail current of nine times I44. But the input currents are reduced by one-nineth. The gain of the first stage is $A_{V1} = V_T R1/(I44 + I60)/2 = 20$.

The offset voltage of this stage is now dependent on six transistors, Q1, Q2, Q3, Q4, Q58, and Q59. However, careful layout results in a typical V_{OS} of 200μV. Zener trim on the load resistors allows further improvement at wafer sort[1].

Having achieved this low error input stage, it must be protected from degradation by succeeding stages. Level shifting now with standard process zener diodes will cause high levels of noise and drift[2]. So, before level shift, another gain stage (A_V = 25) is used. This requires careful biasing of the first two stages to prevent saturation. The voltage levels of these stages are dependent on NPN current sources, diffused resistors, and schottky diodes. The bias network of I62, I45, Q39, Q41, R23, R24, S5, S6, and S9 provide a process and temperature tracking bias that provides the maximum input common mode range and guarantees no saturated devices.

With a gain of 500 in front of the level shift, surface zeners are more than adequate for the job. The level shift gain is approximately 0.85.

A TTL output stage requires an unbalanced swing. The base of the output device, Q19, must be rapidly charged and discharged. The voltage swing at the base only needs to be a few hundred millivolts. However, the collector of Q19 must swing several volts.

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These requirements are met by the output stage of the 4805. A current source, I71, is steered by Q68 and Q69 to either provide rapid discharge of Q19's base or to increase the pulldown current at the comparator output. This current switched output stage provides fast, symmetrical switching rates. Figure 2 shows the 4805 propagation delay for 5mV, 2.5mV, and 1.2mV overdrives.

The TTL compatible latch overrides the inputs, locking the output in whatever state existed when the latch was enabled. This is accomplished by switching I60 from parallel input stage pair Q58, Q59 to differential pair Q56, Q57. Q56, Q57 monitor the output state. They are connected to the collectors of Q58, Q59 but provide positive feedback. Matching n-V_{BE} level shifts provide bias for the latch current switch pair, Q54, Q55. The input voltage to the switch is schottky clamped by S7 and S8.

The time from latch release to output release, or the latch disable time, is 22nS. The latch enable time, or the time the input signal must be available to be correctly latched is 16nS. See Figure 3.

The 4805 is a very wide bandwidth device, having 30dB of gain at 100MHz (Figure 4). Care must be taken during circuit layout to minimize feedback from parasitic capacitance[3]. This is especially important for high value source resistors ($R_S > 1K\Omega$). The use of a ground plane is recommended. Figure 5 shows the 4805 pin assignment. A ground trace from pin 1 to pin 5 (and pin 6 if the latch isn't used) helps reduce oscillations. Lead dress and adequate bypass is critical.

Analog-to-Digital Conversion

A comparator is actually a one bit A-to-D converter. So, it is understandable that major emphasis is placed on analog-to-digital conversion applications for comparators.

The dominant techniques for data conversion above instrumentation frequencies are successive approximation and parallel flash. Successive approximation (SA-A/D) is primarily used for high resolution (> 8 bits) at moderate speeds (< 1MHz). Parallel flash converters operate at lower resolutions (< 10 bits) and high speeds (> 10 MHz)[456].

Successive approximation conversion is accomplished by comparing each bit, starting with the most significant, to an input voltage. Figure 6 shows the typical block diagram. The comparator examines the difference between the trial bit and the input. If the addition of the bit causes the trial value to exceed the input, the bit is complemented. If the trial value remains below the input, the bit is retained. This procedure is repeated for each bit. The converted output is available after N trials. For a trial time of T_1, the conversion time using this method is $(N + 1)\ T_1 = T_C$.

A caution here is warranted. During T_C the input must not change more than one half the value of the least significant bit (LSB). Larger changes will cause errors in the output. This restraint greatly limits the potential bandwidth of a SA-A/D converter.

As an example consider a hypothetical 10 bit, 10μS converter with a 10 Volt input range. One half LSB of this system is 4.9 millivolts. The maximum slew rate of an input signal is 4.9mV/10μS. This would apparently limit the maximum frequency of a full power input signal to 15.6Hz.

This drawback is remedied by the use of a sample and hold amplifier (S/H) at the input to the converter. The S/H, also known as a track and hold, follows the input until switched to the hold mode at time T_O. The output is then a DC value equal to the input at T_O. The S/H introduces its own errors but the primary influence is due to the time required to acquire a new signal at the completion of the SA-A/D conversion. This means that the effective conversion time is actually $T_C' = T_C + T_{ACQ}$. For tips on S/H selection, see reference[4].

The time required for each trial is the sum of three separate events

The DAC Settling Time
The Comparator Progapation Delay
The Logic Delay.

The first two parts are actually interrelated. High speed current output monolithic DAC's have an output capacitance of 20pF to 30pF. The time constant formed by that capacitance and the sum node equivalent resistance dominates DAC settling time for $R_{EQ} > 500\Omega$ (Figure 7). So lower output impedance improves DAC settling time. However, the overdrive to the comparator is decreased by lower output impedance (Figure 8). As long as overdrive to the 4805 is > 1mV, comparator propagation time changes very little.

The logic delay time can be tailored by the user by choosing from either low power or standard TTL versions of the successive approximation register, 2502, 2503, 2504. Higher speed can be obtained from the users own gate level design using schottky TTL[4].

A detailed schematic of a 12-bit SA-A/D converter is shown in Figure 9. It is designed for a 0v to 10V input range. By connecting bipolar offset resistor R3, the input range becomes ±5V. In both cases, the most negative input is represented by 000 000 000 000; the most postive input results in output code 111 111 111 111. This may be complemented by reversing the comparator inputs and using $\overline{I_O}$ rather than I_O of the DAC. R6, R7, and R8 provide an offset of 1/2 LSB. This places the code transistion in the center of the nominal code value; eliminating a DC offset when the analog signal is reconstructed.

Clampling schottky diodes on the sum node protect the comparator inputs from over voltage and decrease the number of time constants required to settle. R9 is selected to minimize errors due to comparator input bias currents. R9 should be equal to the equivalent resistance at the sum node.

R2 is an optional resistor. It may be used to reduce R_{EQ} and therefore the DAC settling time. However, as discussed above, this also reduces comparator overdrive. In this 12-bit design, the comparator overdrive, or 1/2 LSB of the DAC, is 1.22mV. Any further reduction of this overdrive will cause excessive comparator delay. So, in this particular design, R2 is not used. However, if a functionally similar DAC of higher output current or lower resolution is substituted for the 6012, R2 may be used to increase the conversion rate.

Monotonicity was maintained to clock rates as high as 2MHz. Excellent step size uniformity was obtained with a 1.6MHz clock. This results in an 8μS 12-bit conversion for only $40 in parts cost, at 100 piece prices.

Parallel flash conversion provides the highest speed conversion. The input signal range is divided up into $2^n - 1$ discrete levels. A comparator is referenced to each of the levels. The input is applied simultaneously to each comparator input. Logic decodes the "thermometer" type output of the comparators to N-bits. The conversion time is the sum of the comparator propagation delay and the logic decode delay.

Monolithic versions of flash converters have recently become available from several manufacturers in resolutions ranging from 4-to 9-bits. The 4805 can be employed in a flash converter and will allow economical 3- and 4-bit conversion of millivolt level signals at video speeds.

Figure 10 shows the generalized flash converter. The logic decode for the comparator's outputs takes this form:

$$B_1 = C_{2n-1}$$
$$B_2 = C_{2n-2}\,\overline{C_{2(2n-2)}} + C_{3(2n-2)}$$
$$B_3 = C_{2n-3}\,\overline{C_{2(2n-3)}} + C_{3(2n-3)}\,\overline{C_{4(2n-3)}} + \bullet\bullet\bullet$$
$$B_n = C_1\,\overline{C_2} + C_3\,\overline{C_4} + \bullet\bullet\bullet + C_{2n-3}\,\overline{C_{2n-2}} + C_{2n-1}$$

This is readily implemented using standard TTL functions for $N \leq 4$ (Figure 11).

A three bit flash was built according to the schematic in Figure 12. Schottky TTL was used for minimum propagation delay. A 20mV peak to peak signal was converted at a 20MHz rate. For larger signals, the conversion rate can be increased to 25MHz.

An interesting application for such a converter is speeding up a SA-A/D conversion (Figure 13). The 12-bit converter in the earlier example can be terminated after 8- or 9-bits. The remaining bits can be encoded in a fraction of a clock cycle by flash converting the remainder present at the sum node. The reference voltage for the flash converter equals the new LSB of the truncated SA-A/D. This provides a conversion time 70% to 77% of the standard procedure.

Precision Latching Window Comparator

The window comparator is a common function performed by comparators. It is an ideal application to demonstrate the versatility that the 4805's speed, precision, and latch allows.

Settling time measurement on DACs and Op Amps is a time consuming job requiring a skilled technician. The 4805 easily enables

GO/NO GO testing to 0.1% of 10 volt steps, 250nS settling times with less than 10% measurement error.

Figure 14 shows the basic window comparator and its state table. Figure 15 uses the basic configuration and a time delay to indicate Pass/Fail on settling time. Outputs B and C are tied back to their own latch enables. The latch inputs are forced low by the one shot until the DUT is presumed to be settled. When the one shot releases the latch, the comparator outputs will hold the latch off as long as the input remains in the specified range. Output A can be queried by ATE equipment or can drive an operator monitored indicator. The DUT should be biased to settle to ground. Diode clamps at the window comparator input protect against over-voltage. They may be omitted for small value pulses.

The Raytheon 4805 provides a new high performance tool for the system designer. Its capabilities are far greater than that covered by the above examples. The low cost of this high performance comparator will generate many additional uses in a wide variety of system applications. Figures 16 through 19 show additional performance characteristics. The pad locations of the 3,400 square mil. chip are shown in Figure 20.

[1] G. Erdi, "A precision trim technique for monolithic analog circuits," IEEE J. Solid-State Circuits, Vol. SC-10, pp 412-416, Dec. 1975.

[2] ....., "A Fast, Latching Comparator for 12-Bit A/D Applications,"IEEE J. Solid-State Circuits, Vol. SC-15, No. 6, pp 949-954, Dec. 1980.

[3] L. Brown, "Am685/Am686/Am687 Designing with High Speed Comparators," Linear and Interface Data Book, Advanced Micro Devices, Sec. 2, pp 48-57, 1979.

[4] W.G. Jung, "IC Converter Cookbook," H.M.SAMS and Co., 1978

[5] W.K. Bucklen, "The Industry's First Monolithic Nine-Bit Flash A/D Converter," Electronic Design Week Conference Proceedings Linear IC Applications, Vol. L3, pp 366-390, 1981.

[6] B.M. Gordon, "Linear Electronic Analog/Digital Conversion Architectures, Their Origins, Parameters, Limitations, and Applications," IEEE Trans. Circuits and Systems, Vol. CAS-25, pp 391-418, July 1978.

Table 1. Features and Specifications
(Vs = ±5V, TA = 25°C unless otherwise specified)

Input Offset Voltage	-55°C ≤ TA ≤ +125°C	250μV Max 800μV Max
Input Offset Current	-55°C ≤ TA ≤ +125°C	80nA Max 200nA Max
Input Bias Current	-55°C ≤ TA ≤ +125°C	1.2μA Max 2.5μA Max
Propagation Delay	100mV Step, 5mV O.D. -55°C ≤ TA ≤ +125°C	35nS Max 50nS Max
Power Dissipation	Vo ≤ 0.4V -55°C ≤ TA ≤ +125°C	160mW Max 190mW Max
Latch Enable Voltage High	-55°C ≤ TA ≤ +125°C	2.0V Min
Low	-55°C ≤ TA ≤ +125°C	0.8V Max
Input Voltage Range	-55°C ≤ TA ≤ +125°C	±2V Min
Voltage Gain		20,000 Typ
Power Supply Range Positive		4.5V to 5.5V
Negative		-4.5V to -16.5V
Output Voltage High	Io = 200μA	2.4V Min
Low	Io = -8mA	0.4V Max

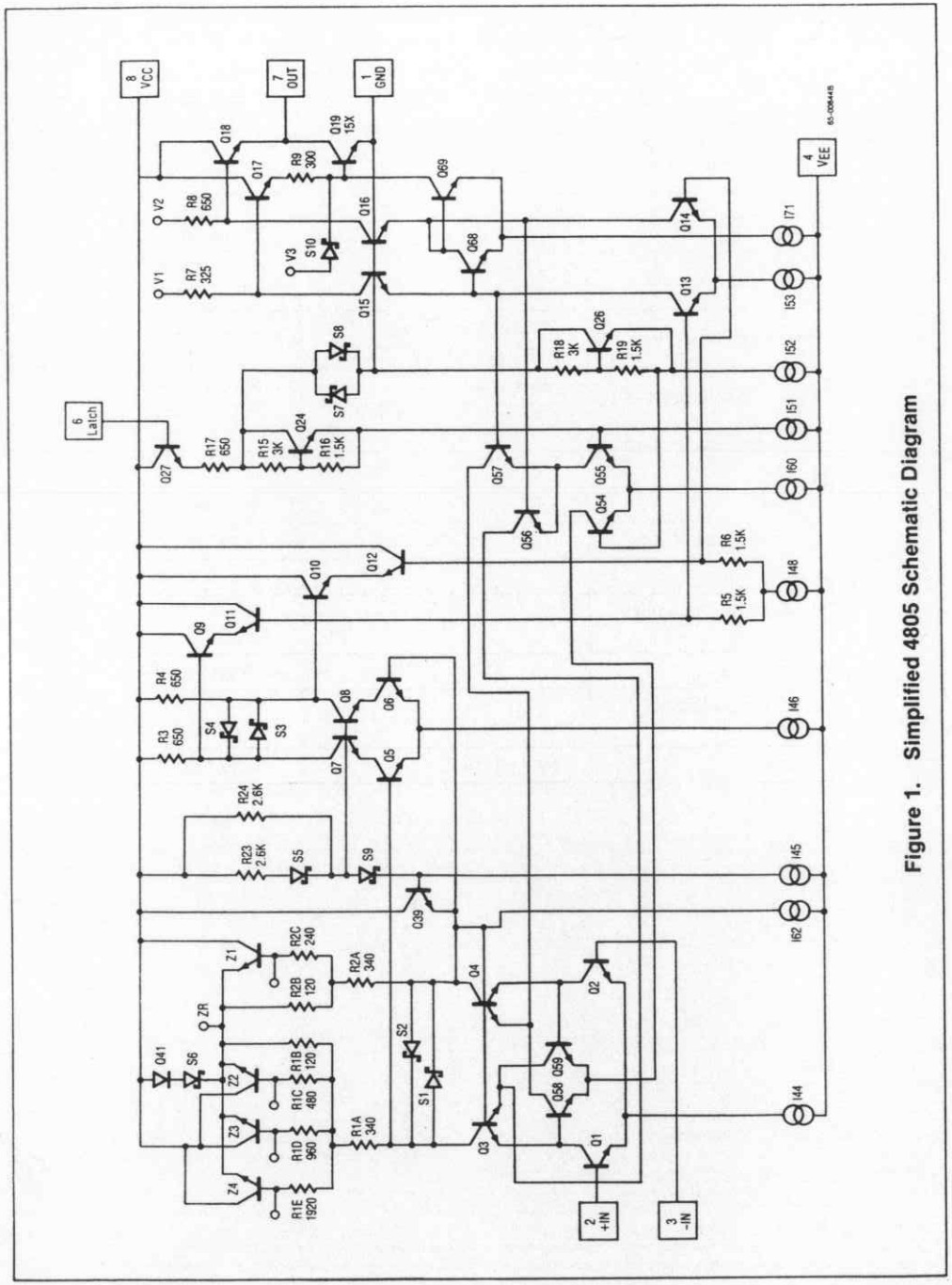


Figure 1. Simplified 4805 Schematic Diagram

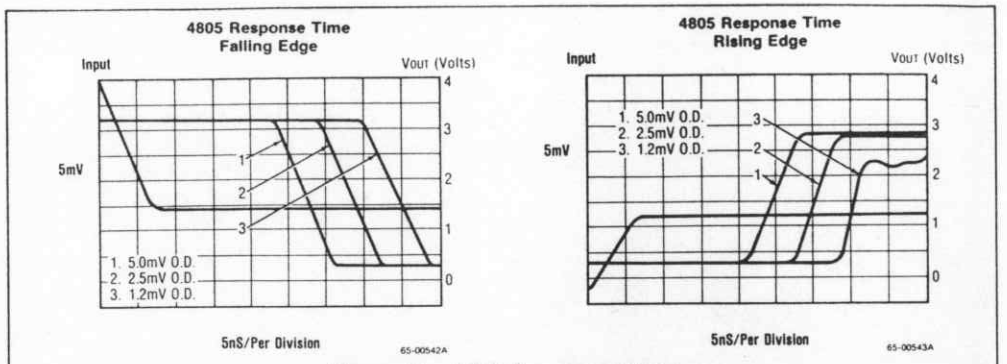


Figure 2. 4805 Response Time

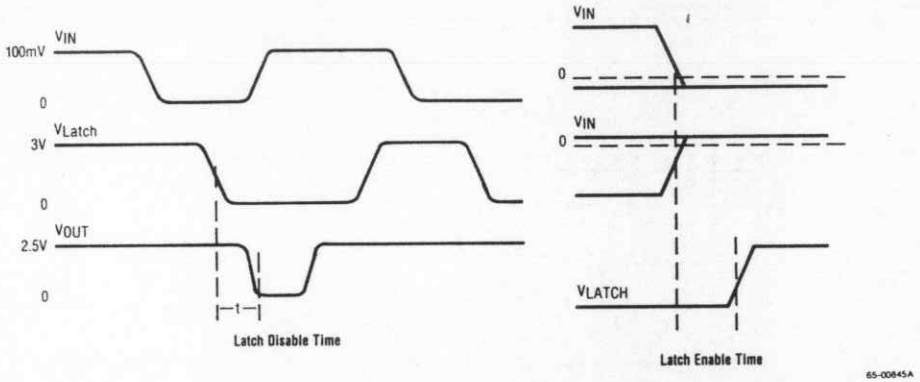


Figure 3. Latch Timing

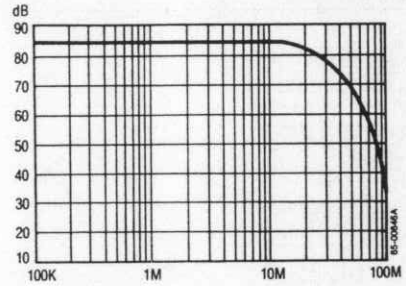
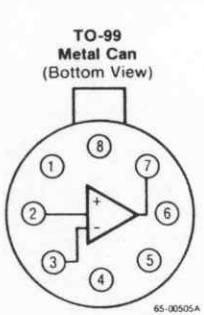
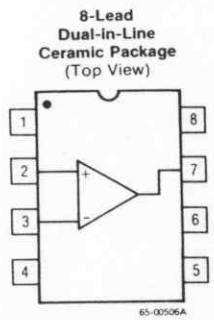


Figure 4. Gain vs Frequency





Pin	Function
1	Ground
2	Non-Inverting Input
3	Inverting Input
4	V-
5	NC
6	Latch Enable
7	VOUT
8	V+

Figure 5. Connection Information

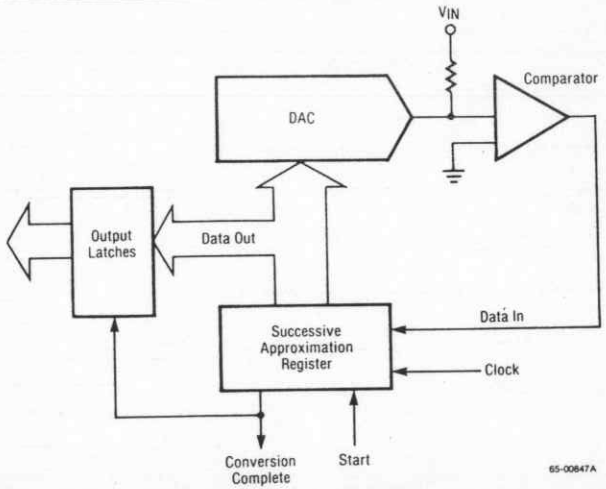


Figure 6. Successive Approximation Block Diagram

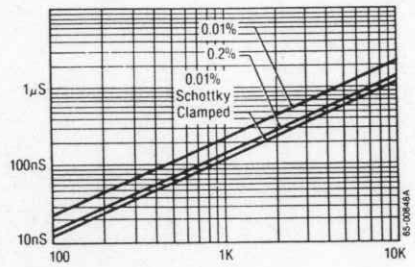


Figure 7. DAC Settling Time vs Sum Node Equivalent Resistance, R_{EQ}

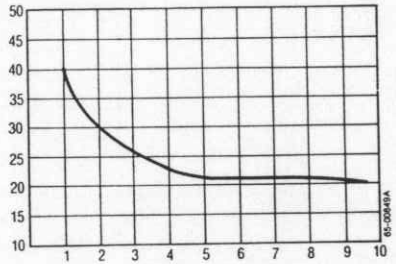


Figure 8. Propagation Delay vs Overdrive, T_A =25° C (V_{IN} = 100mV Step)

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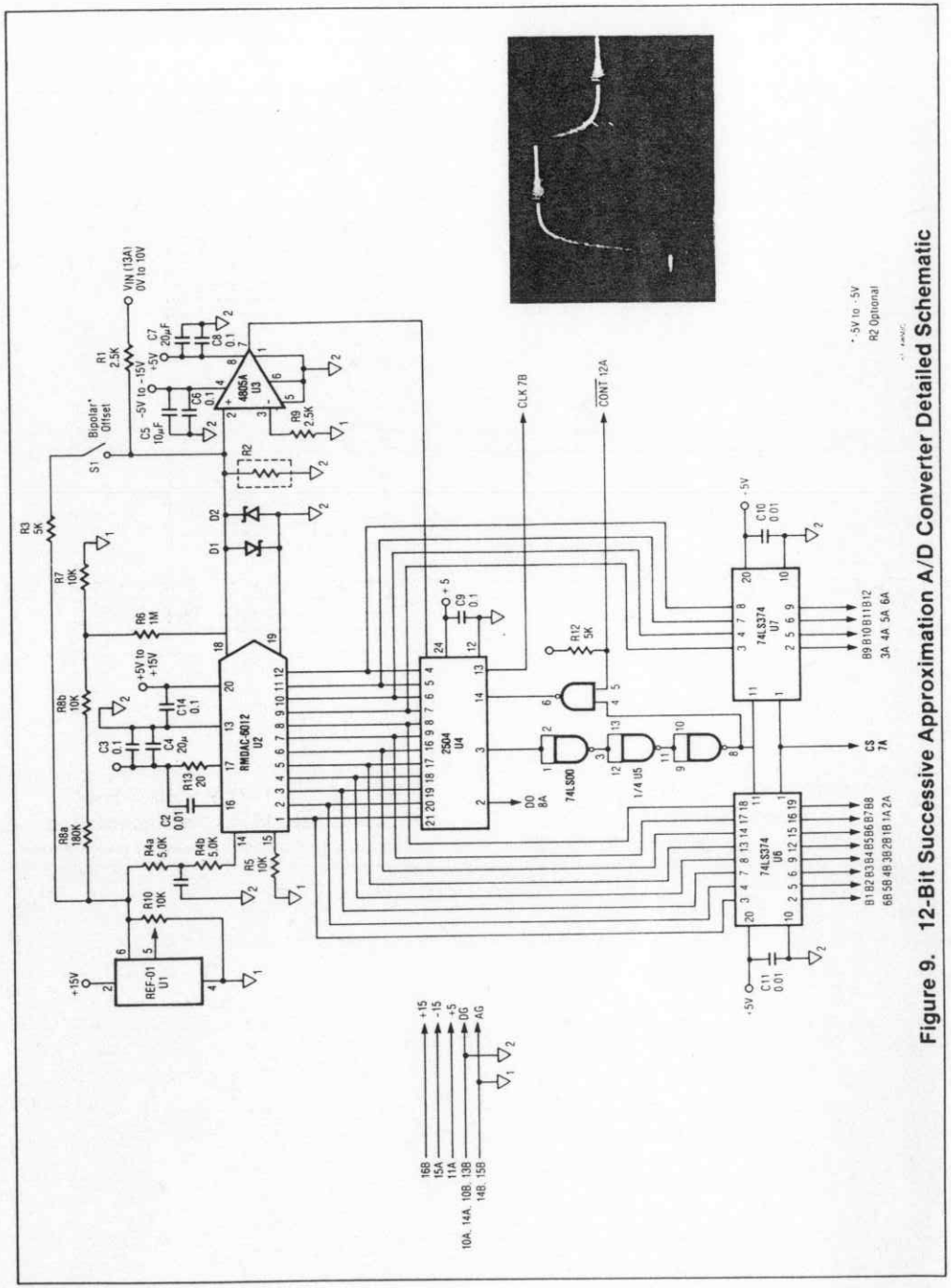

Figure 9. 12-Bit Successive Approximation A/D Converter Detailed Schematic

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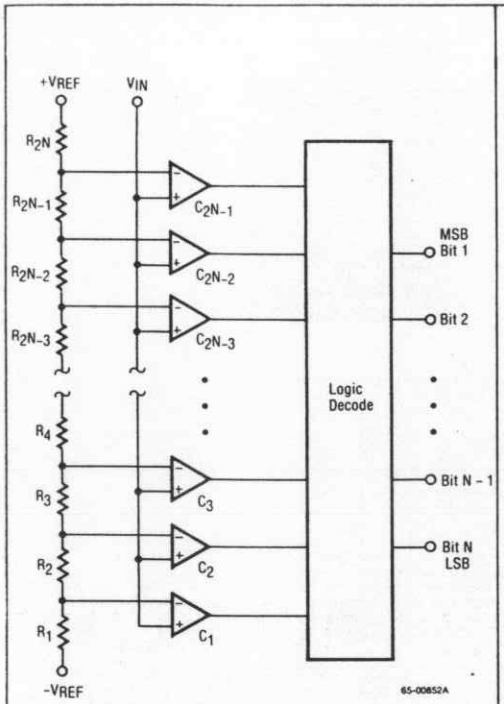


Figure 10. Generalized Flash Converter

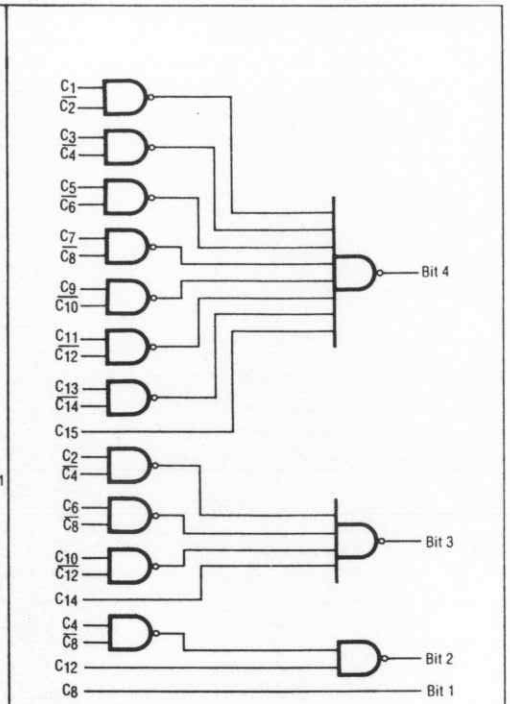


Figure 11. 4-Bit Parallel Flash Logic Decode NAND Implementation

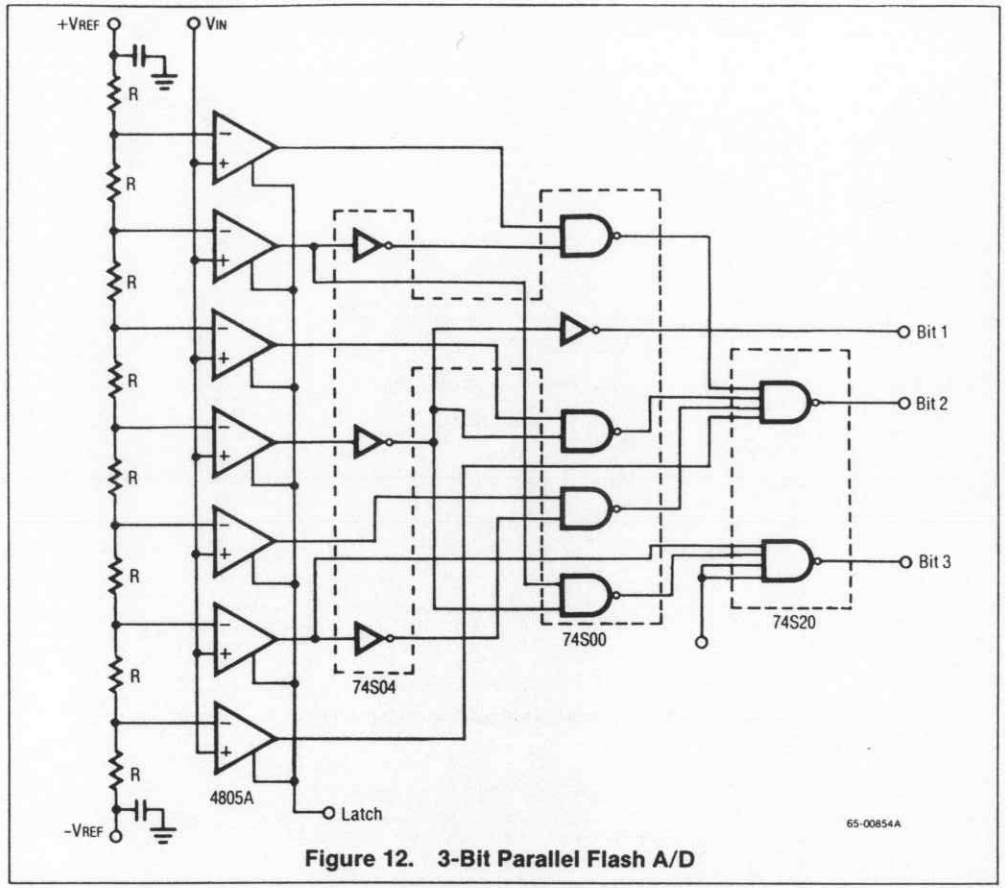


Figure 12. 3-Bit Parallel Flash A/D

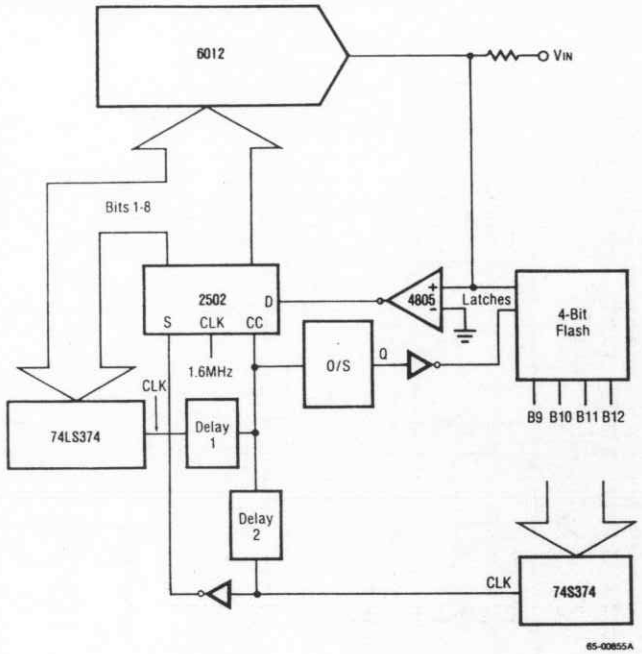
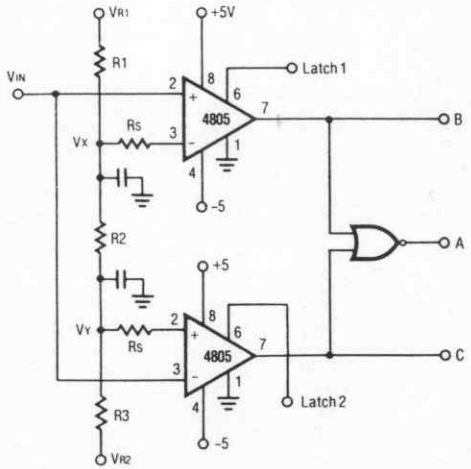


Figure 13. 12-Bit Successive Approximation/Flash Converter



VIN (VX > VY)	A	B	C
VIN > VX	0	1	0
VX > VIN > VY	1	0	0
VY > VIN	0	0	1

Figure 14. Precision Latching Window Comparator

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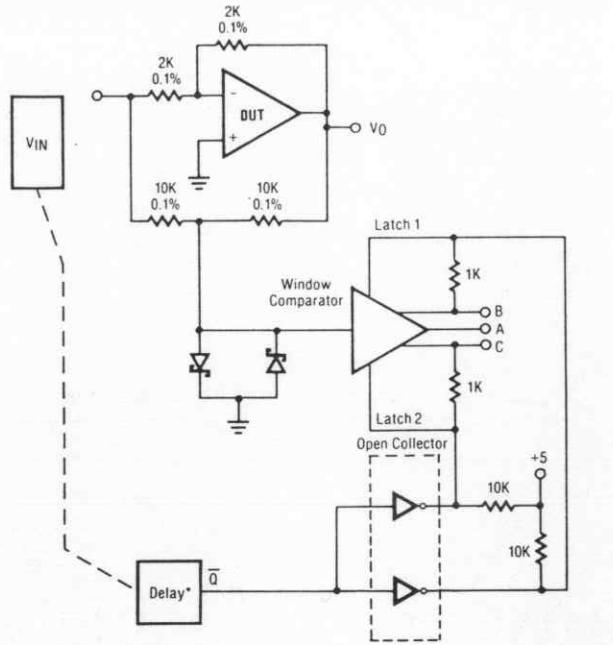

*Delay should equal the settling time specification minus 30nS minus appropriate guard band

Figure 15. Settling Time Tester

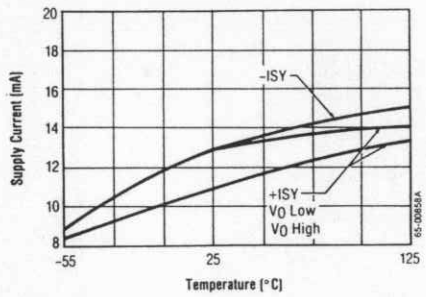

Figure 16. Supply Current vs Temperature

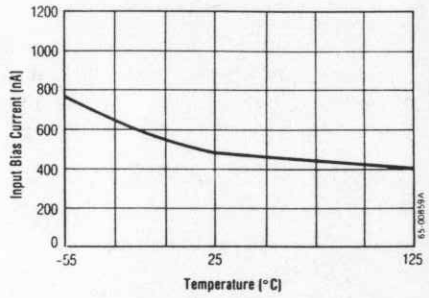

Figure 17. Input Bias Current vs Temperature

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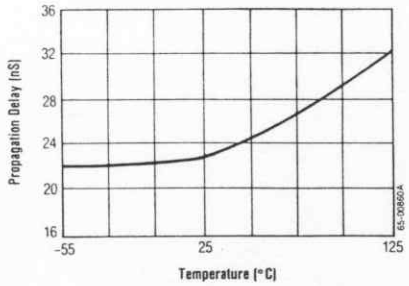


Figure 18. Propagation Delay vs Temperature

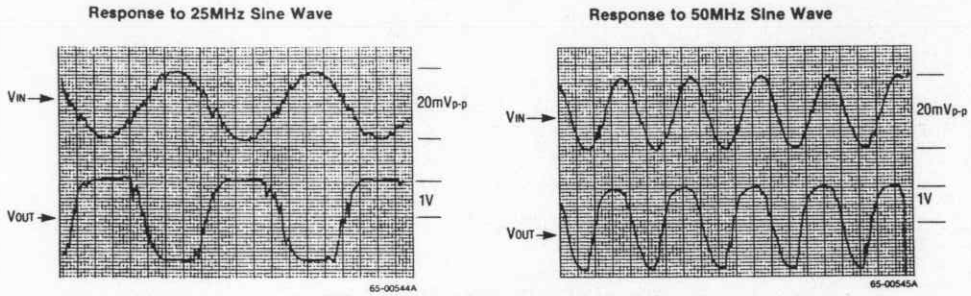
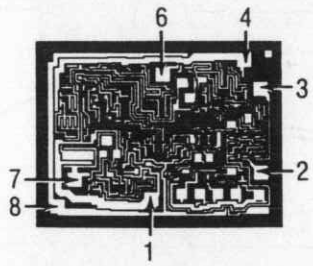


Figure 19. Response to Sine Wave



Die Size: 51 x 67 mils
Min. Pad Dimensions: 4 x 4 mils

Figure 20. Mask Pattern

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